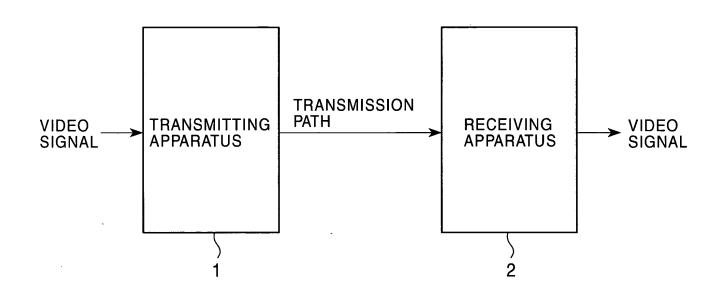
FIG. 1





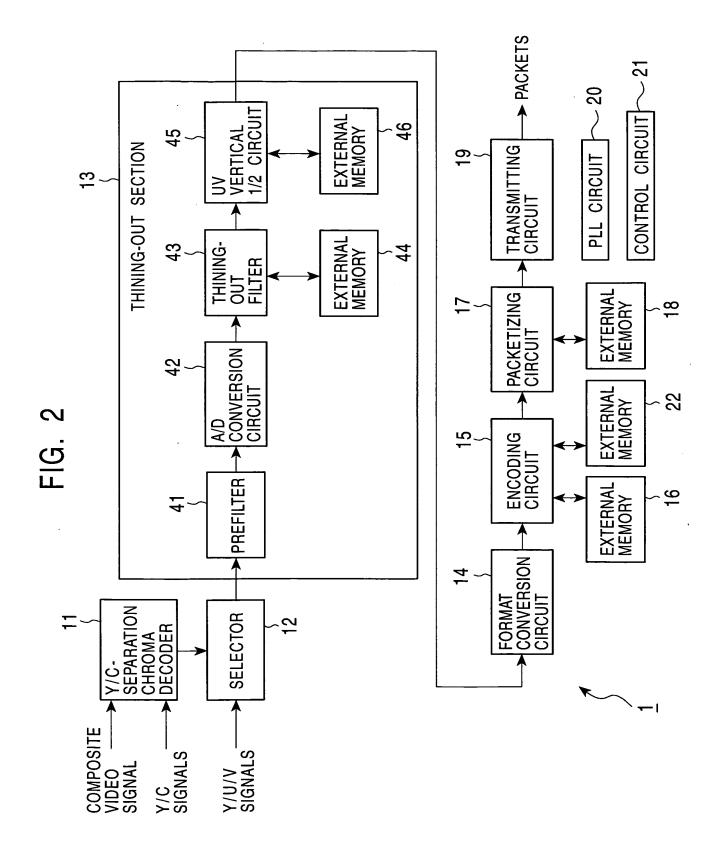
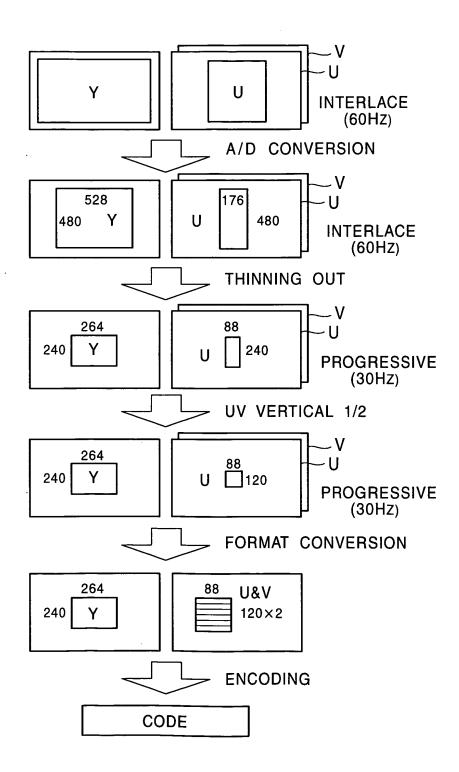


FIG. 3



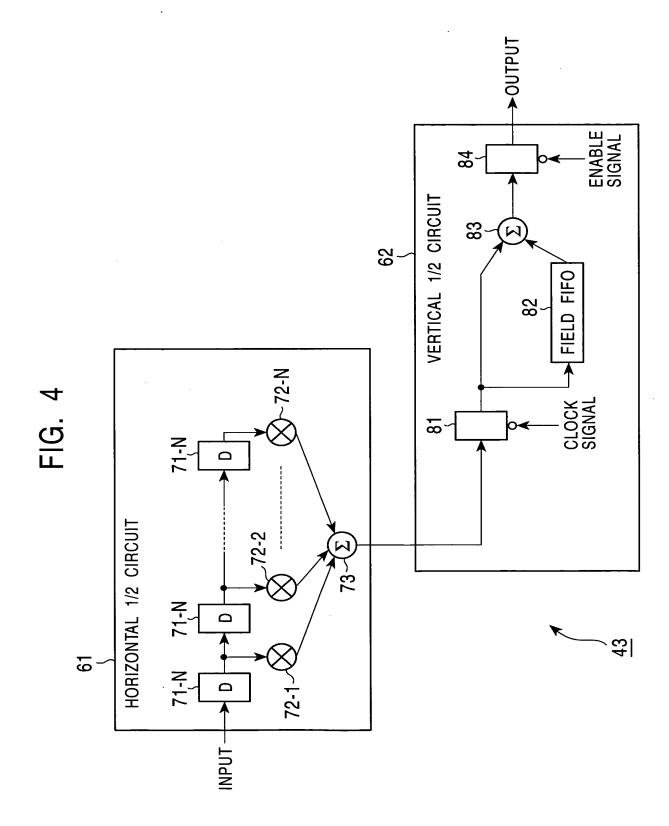
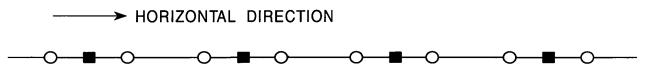


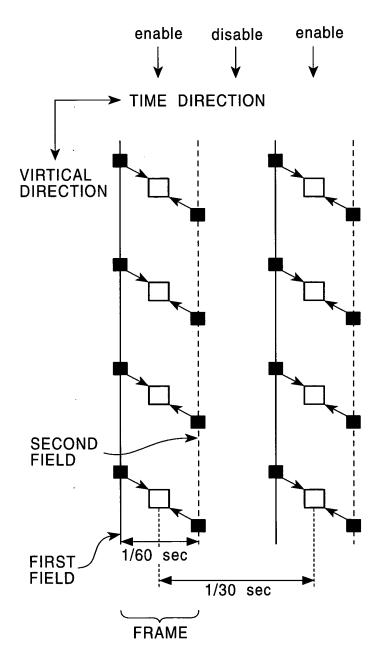
FIG. 5



O PIXELS INPUT TO HORIZONTAL 1/2 CIRCUIT

■ PIXELS OUTPUT FROM LATCH CIRCUIT 81

FIG. 6



- PIXELS OUTPUT FROM LATCH CIRCUIT 81
- PIXELS OUTPUT FROM LATCH CIRCUIT 84

FIG. 7

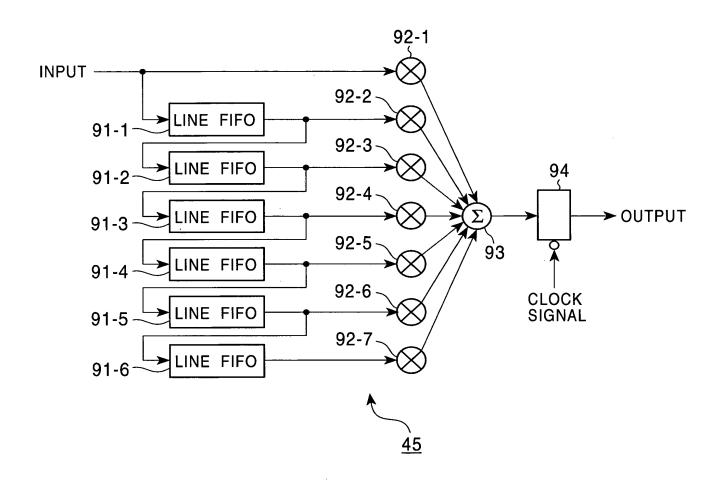
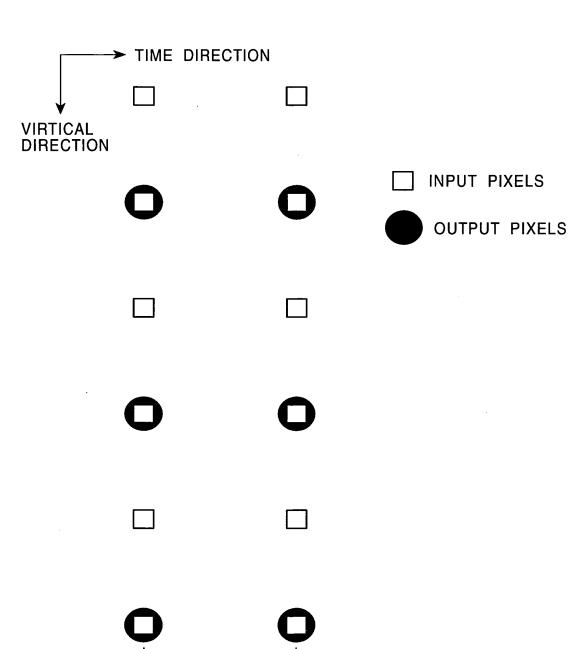


FIG. 8



1/30 sec

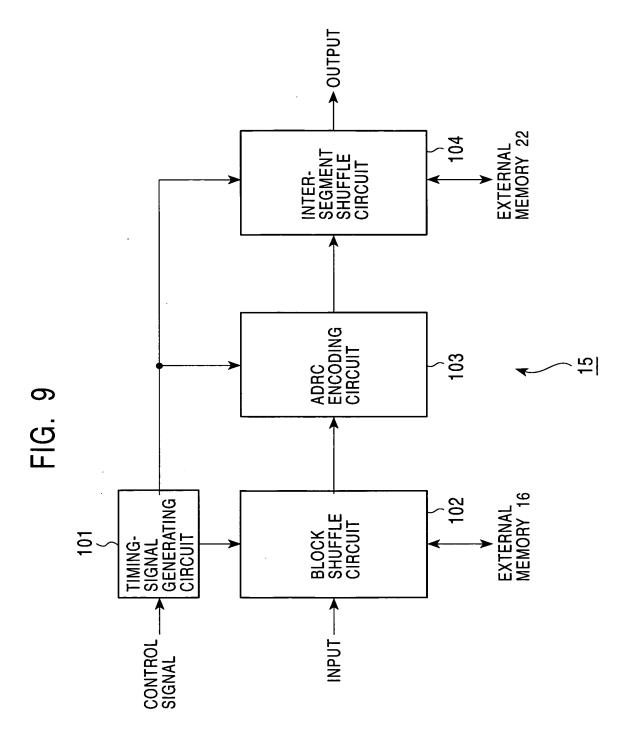
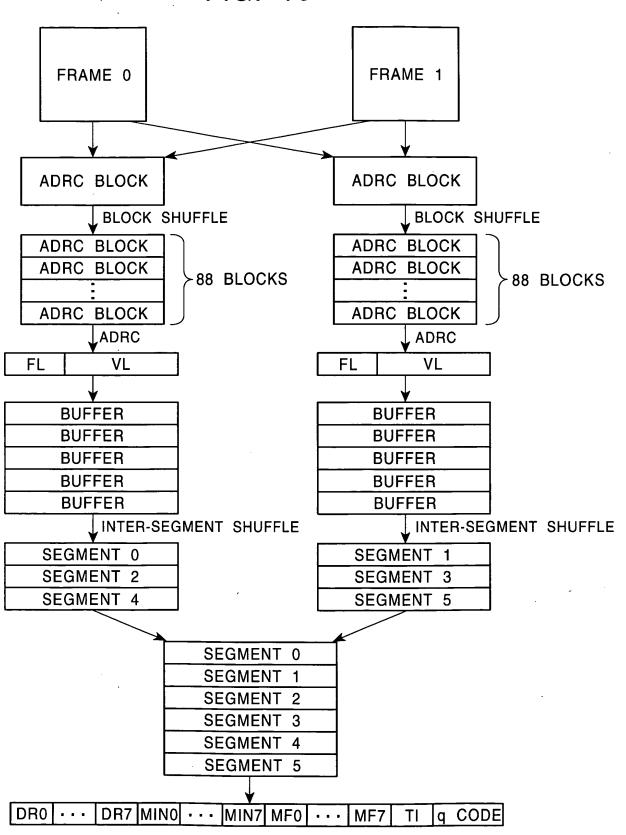
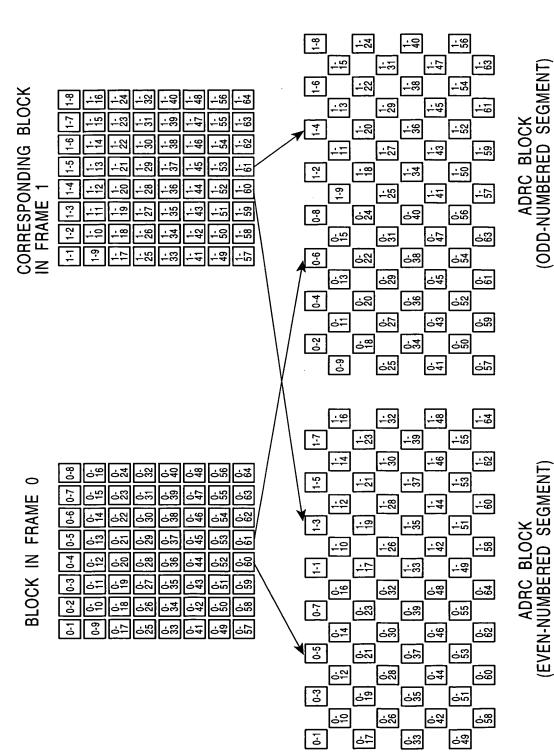


FIG. 10





ADRC BLOCK (EVEN-NUMBERED SEGMENT)

FIG. 12

FRAM	E 0	33 BLOCKS				
8 PIXELS	8 PIXELS \		8 /PIXELS	8 YPIXELS \		
A1	A2		A32	A33	8 PIXELS	
B1	B2	• • •	B32	B33	8 PIXELS	
C1	C2		C32	C33	8 PIXELS	
A34	A35		A65	A66	8 PIXELS	
B34	B35		B65	B66	8 PIXELS	30
C34	C35	• • •	C65	C66	8 PIXELS	BLOCKS
	• • •			- - -		
A298	A299		A329	A330	8 PIXELS	
B298	B299		B329	B330	8 PIXELS	
C298	C299		C329	C330	8 PIXELS	

FIG. 13

FRAM	E 1	—— 33 BLOCKS ——				
8 PIXELS	8 YPIXELS		8 PIXELS	8 γPIXELS γ		
A1	A2		A32	A33	8 PIXELS	
B1	B2		B32	B33	8 PIXELS	
C1	C2		C32	C33	8 PIXELS	j
A34	A35		A65	A66	8 PIXELS	
B34	B35		B65	B66	8 PIXELS	30
C34	C35		C65	C66	8 PIXELS	BLOCKS
	-	 -	-	•		
A298	A299		A329	A330	8 PIXELS	
B298	B299		B329	B330	8 PIXELS	
C298	C299		C329	C330	8 PIXELS	

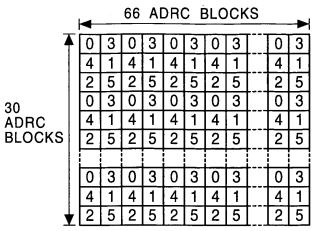
FIG. 14

) OCK	OCK	OCK	OCK	OCK	OCK
ADRC BLOCK	ADRC BLOCK	ADRC BLOCK	ADRC BLOCK	ADRC BLOCK	ADRC BLOCK
ADRC BLOCK 0	ADRC BLOCK	ADRC BLOCK	ADRC BLOCK 0	ADRC BLOCK	ADRC BLOCK
ADRC BLOCK	ADRC BLOCK	ADRC BLOCK	ADRC BLOCK	ADRC BLOCK	ADRC BLOCK
ADRC BLOCK	ADRC BLOCK	ADRC BLOCK	ADRC BLOCK 0	ADRC BLOCK	ADRC BLOCK

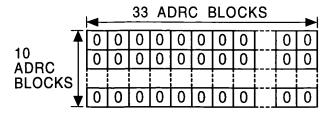
FIG. 15A

FIG. 15B

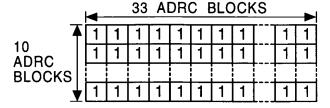




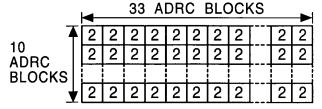
SEGMENT



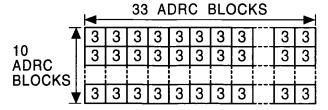
SEGMENT



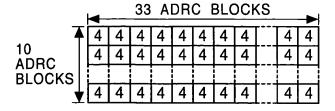
SEGMENT



SEGMENT



SEGMENT



SEGMENT

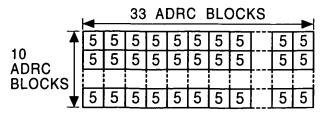
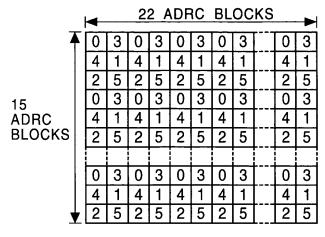


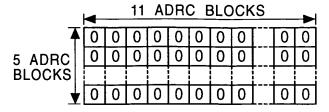
FIG. 16A

FIG. 16B

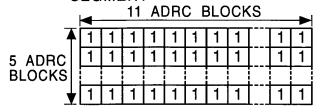




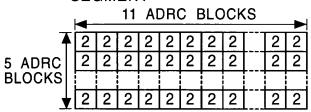
SEGMENT



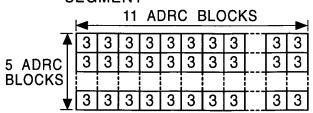
SEGMENT



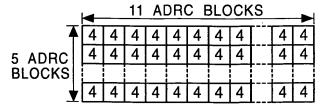
SEGMENT



SEGMENT



SEGMENT



SEGMENT

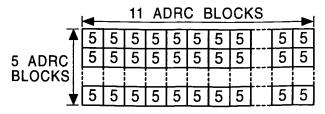


FIG. 17A

y32	396	y329
y4	7 84	y301
у3)36	y300
y2	y35	y299
۲۷	y34	y298
y0	y33	y297

FIG. 17B

y142	y175		y109
y224	y257		y191
у3	y36	!	y300
y112	y145		979
y221	y254		y188
y0	y33		y297

FIG. 17C

u10	u21	n54
u4	u15	u48
n3	u14	u47
n2	u13	 u46
La La	u12	u45
0n	n11	n44

FIG. 17D

n44	n33	0n
n20	6En	 9n
u51	n40	Zn
79n	141	8n
n53	u42	6n
n54	n43	u10

FIG. 17E

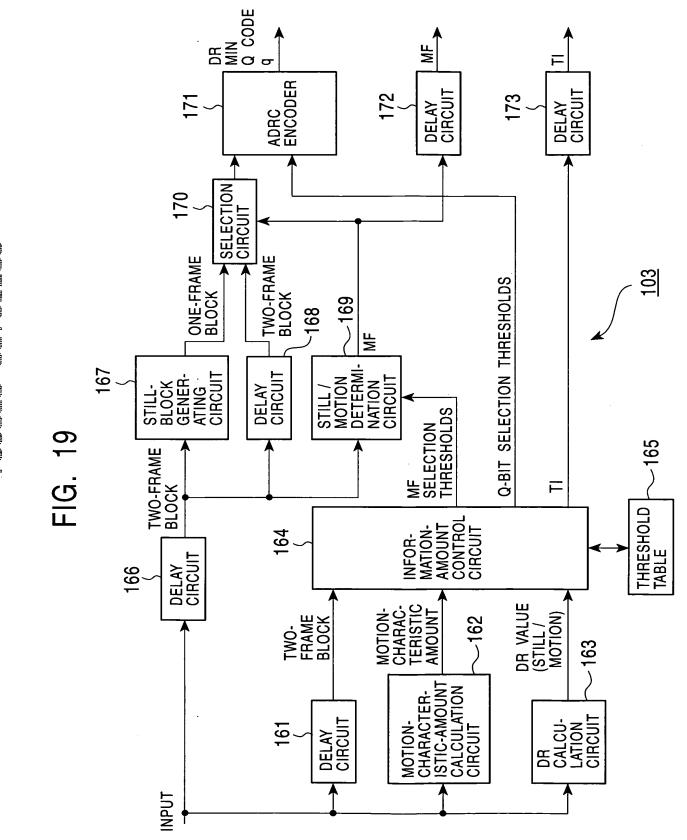
v10	٧21	 v54
٧4	۷15	۷48
٨3	۸14	۷47
۸2	۷13	۷46
١٨	۷12	۷45
۸0	۷11	۷44

FIG. 17F

٧54	v53	v52	v51	v50	۷44
٧43	۷42	۷41	۷40	۸39	٧33
v10	6/	۸8	٧7	9/	۸0

FIG. 18

SEGMENT 5		
SEGMENT 4		0/
SEG		y109 v0
IT 3		
SEGMENT 3		y6
	! !	v54
SEGMENT 2	; ; ;	y115
SEGI		u54 y3 y224 y115 v54 y6
IT 1		уз
SEGMENT 1		n54
S	1	/221 y112
SEGMENT (y221
SEG		y0



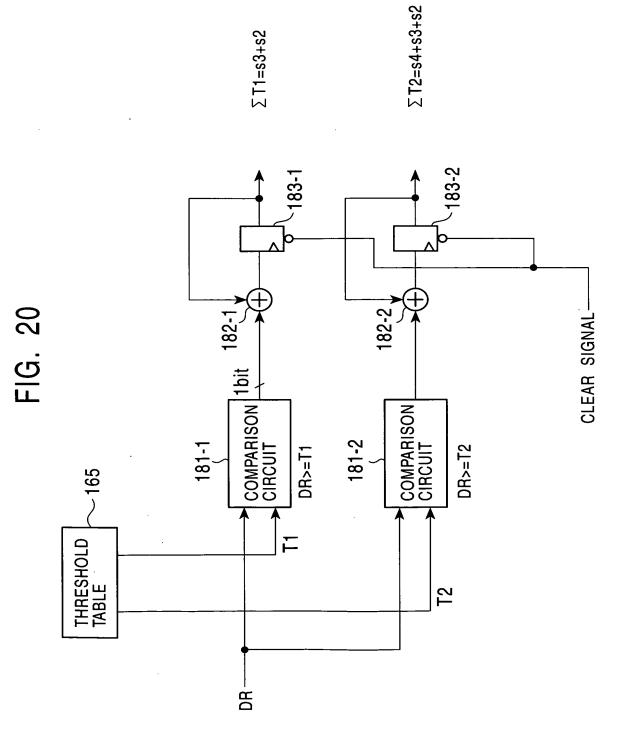


FIG. 21

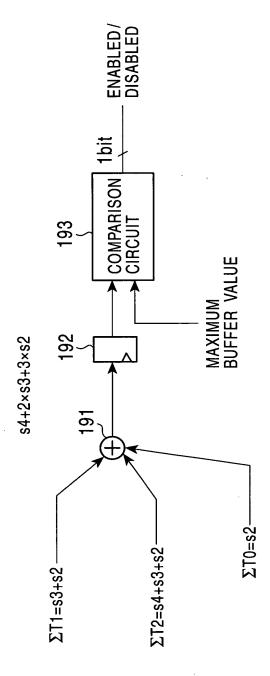


FIG. 22

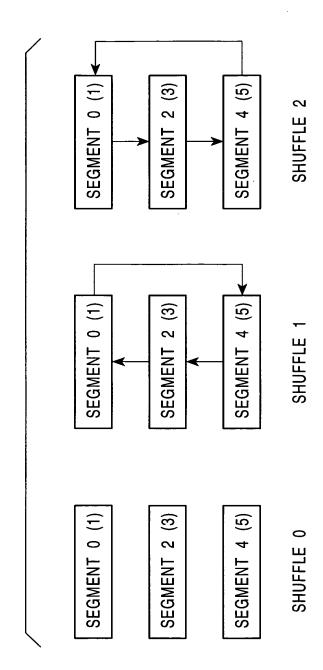


FIG. 23

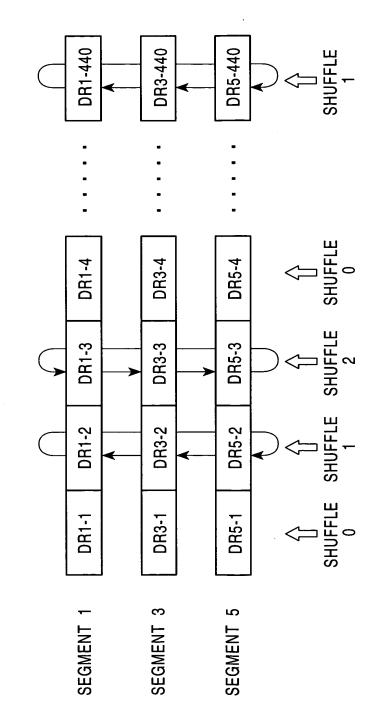
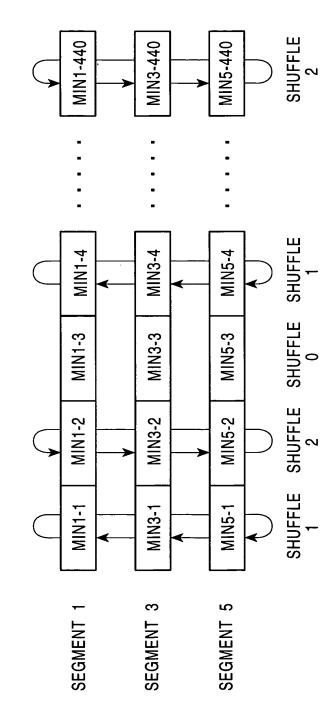


FIG. 24



SHUFFLE 0 MF5-440 MF1-440 MF3-440 SHUFFLE SHUFFLE SHUFFLE 2 MF1-4 MF3-4 MF5-4 MF5-3 MF1-3 MF3-3 MF1-2 MF3-2 MF5-2 MF3-1 MF1-1 MF5-1 SEGMENT 3 SEGMENT 5 SEGMENT 1

FIG. 25

FIG. 26

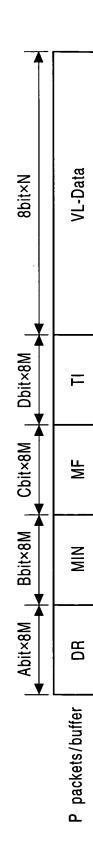
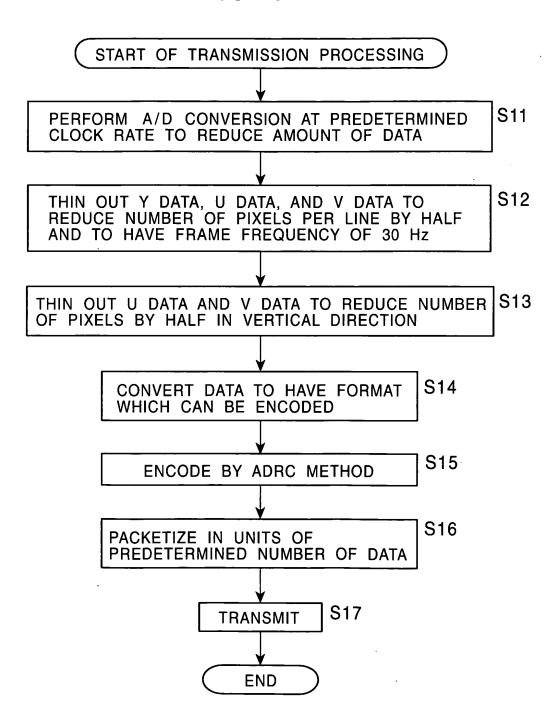
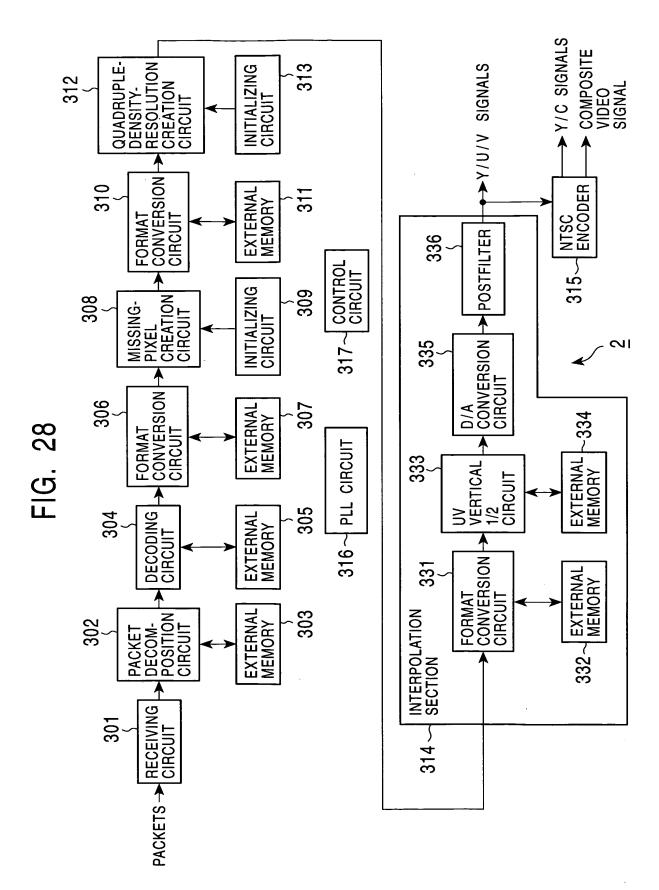


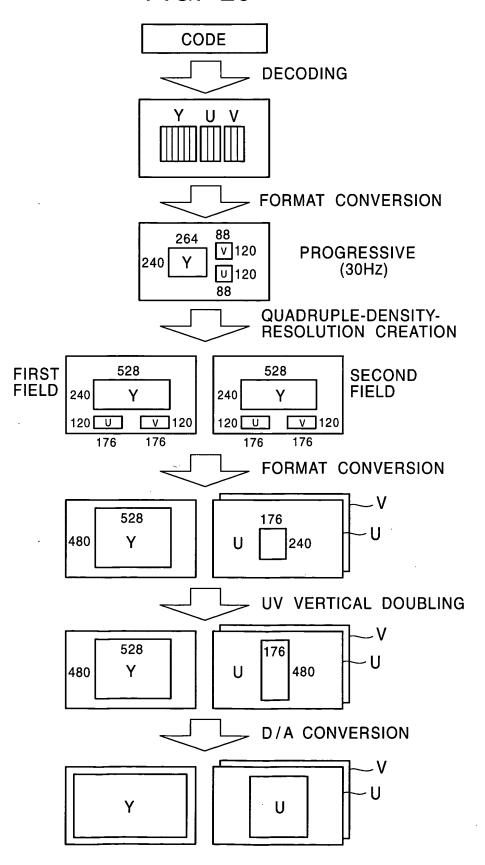
FIG. 27





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FIG. 29



THEILE OF TOTAL

FIG. 31

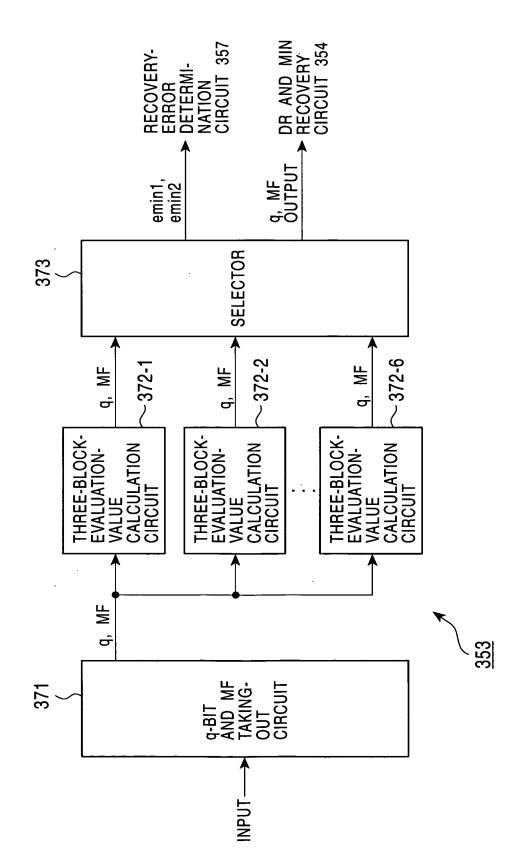


FIG. 32

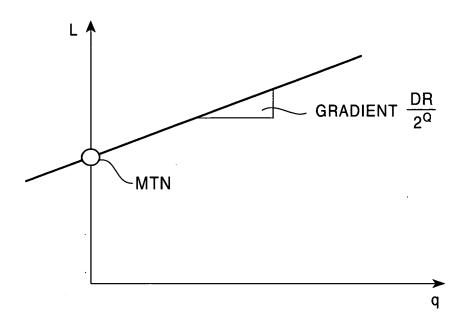


FIG. 33

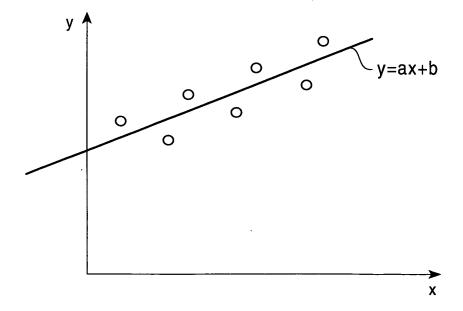


FIG. 34A

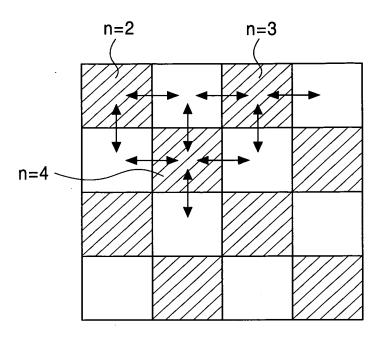


FIG. 34B

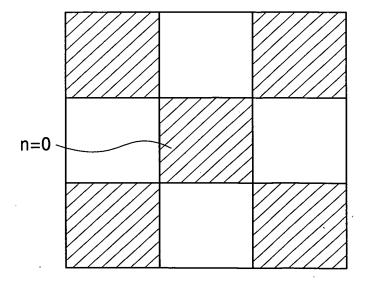


FIG. 35

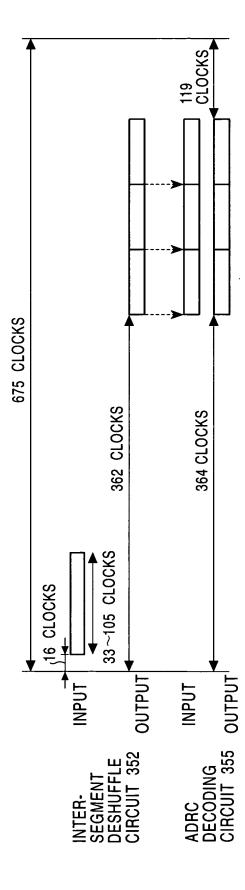


FIG. 36

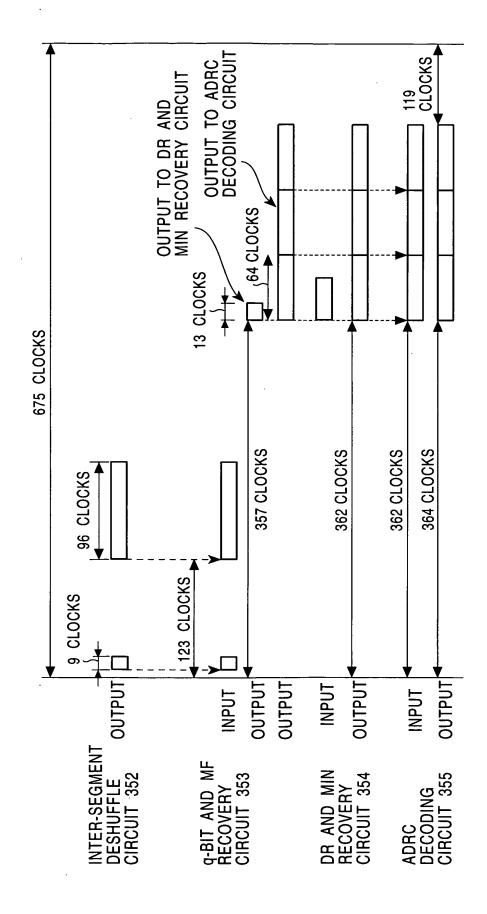


FIG. 37A

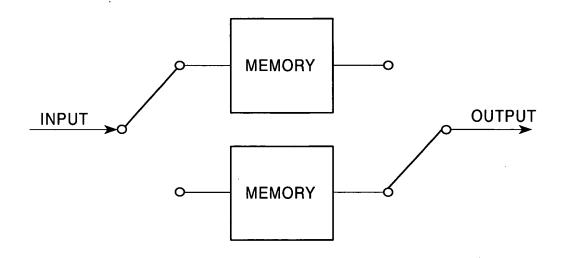


FIG. 37B

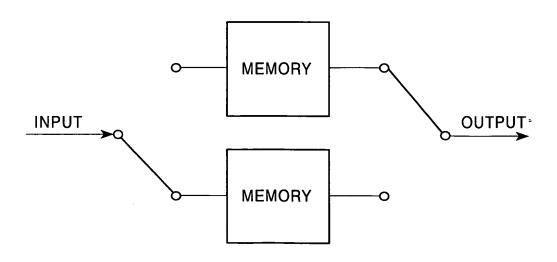


FIG. 38A

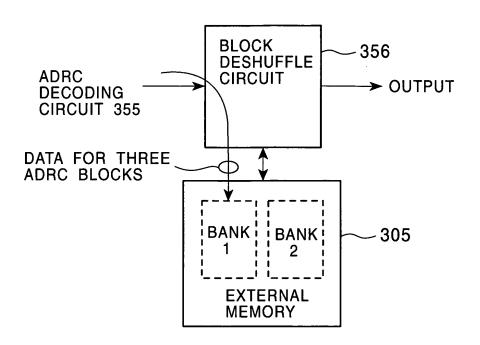


FIG. 38B

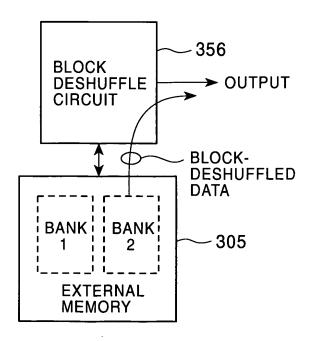


FIG. 39

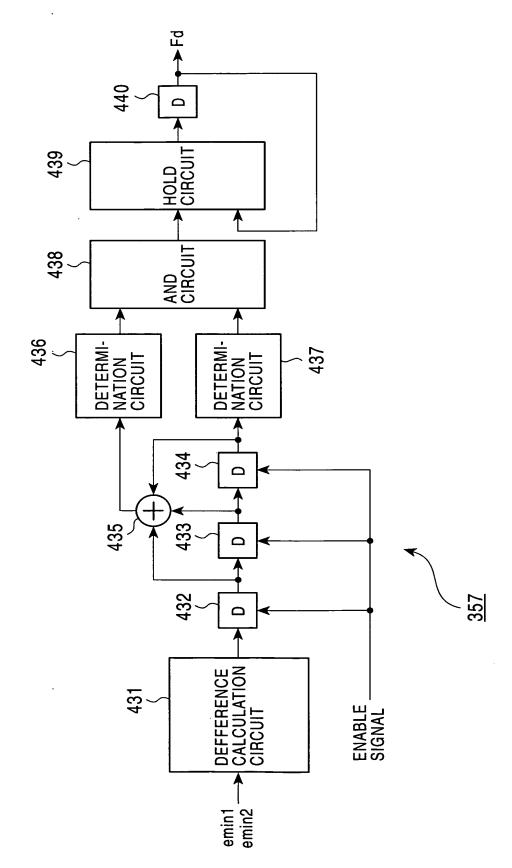


FIG. 40

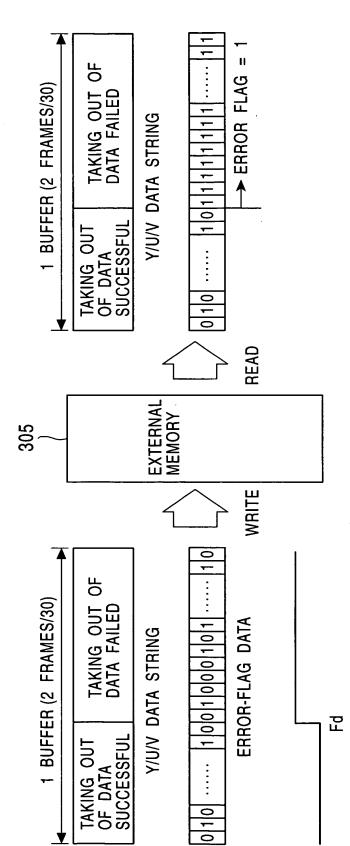
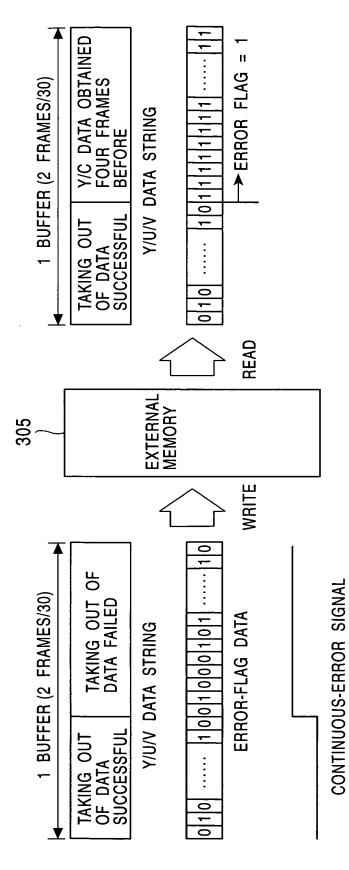
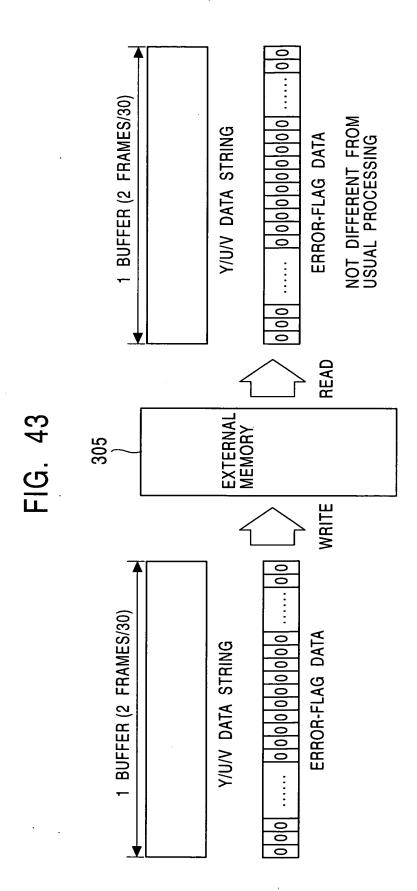


FIG. 41



DECODER WHEN ERROR FLAG IS 1, GRAY IS OUTPUT BLOCK DESHUFFLE CIRCUIT 356 ERROR-FLAG – DATA Y/U/V DATA— STRING READ EXTERNAL MEMORY 305 WRITE 1 BUFFER (2 FRAMES/30) ERROR-FLAG DATA 100100010101 Y/U/V DATA STRING

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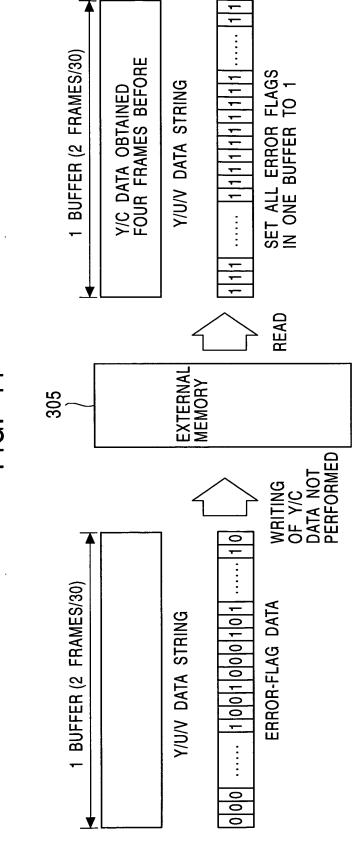


FIG. 44

FIG. 45

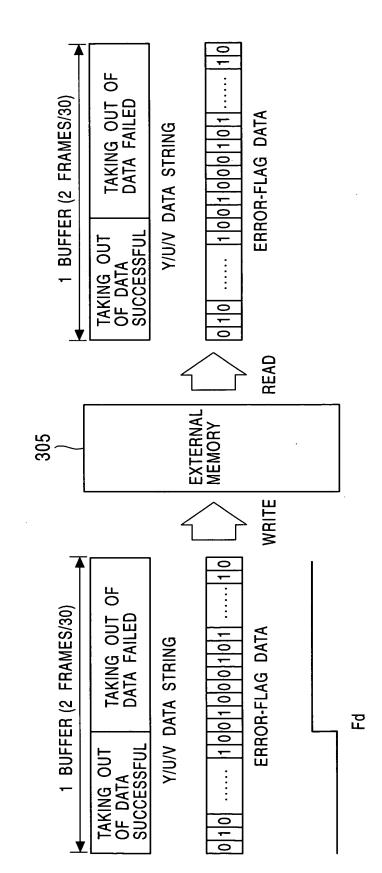


FIG. 46

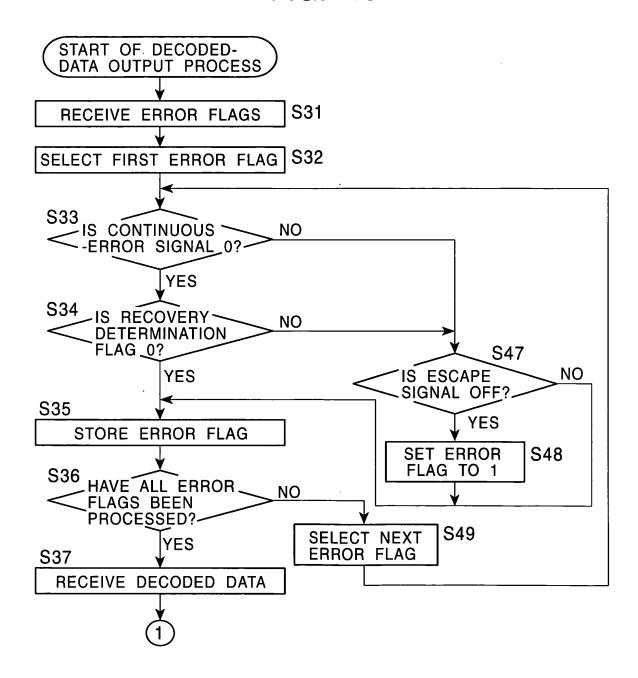


FIG. 47

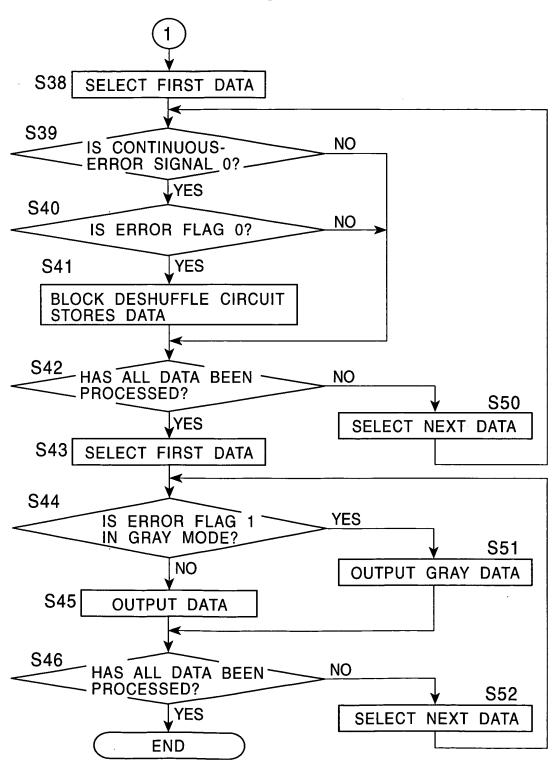


FIG. 48

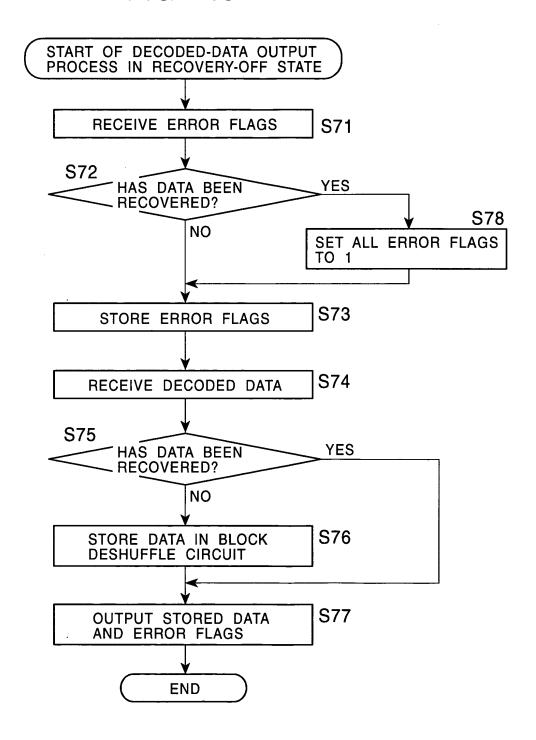


FIG. 49A

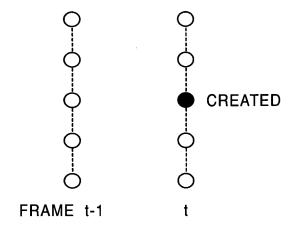
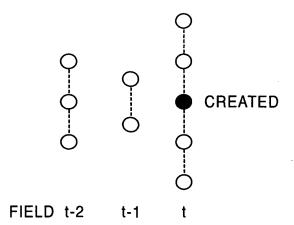


FIG. 49B



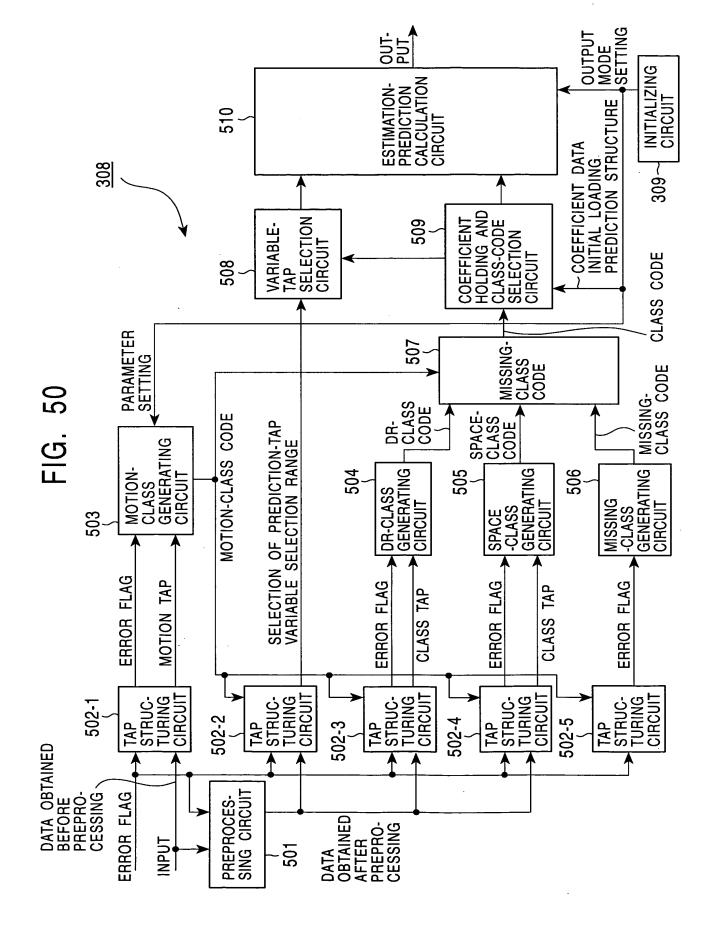


FIG. 51

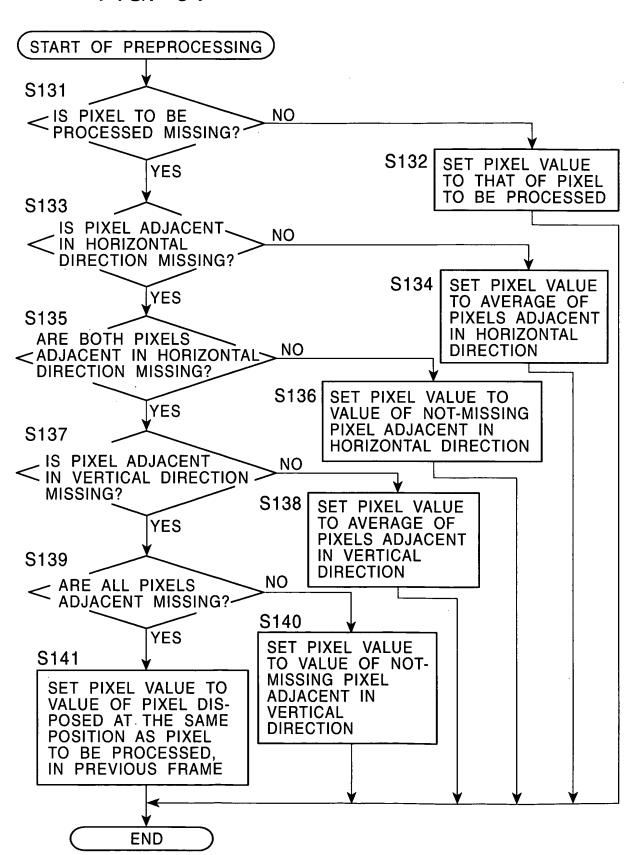


	FIG.	52A			FIG.	52E	3
L1 L2	H1 ERROR q4	ERROR	H3 q3 q6	L1 L2	H1 p1 p4	H2 p2 p5	H3 p3 p6
L3	q7 FRA	ERROR	q9	L3	p7 FRA	p8 .ME t-1	p9

FIG. 53

q1 q2 q3 q4 ERROR q6 q7 q8 q9 FRAME t

FIG. 54

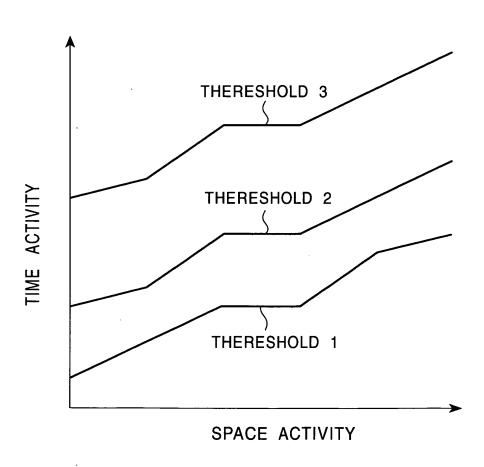


FIG. 55

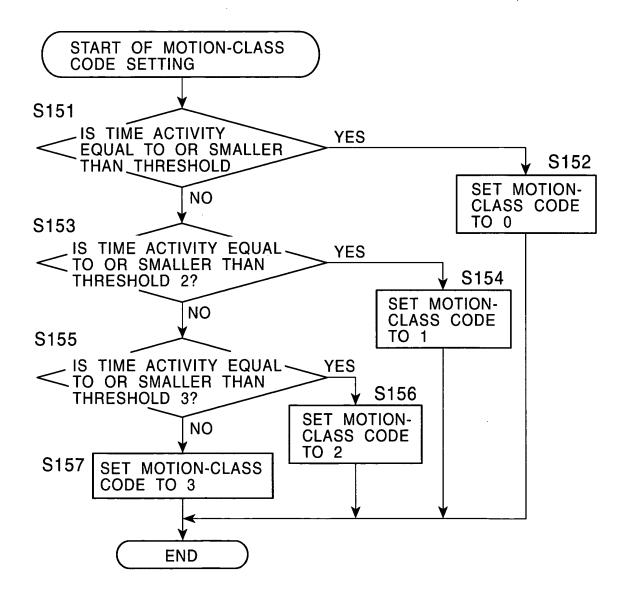


FIG. 56

L-2	\bigcirc	\bigcirc	\bigcirc
L-1	\bigcirc	\bigcirc	\bigcirc
L0	\bigcirc	\otimes	\bigcirc
L+1	\bigcirc	\bigcirc	\bigcirc
L+2			

: PIXEL TO BE PROCESSED

FIG. 57

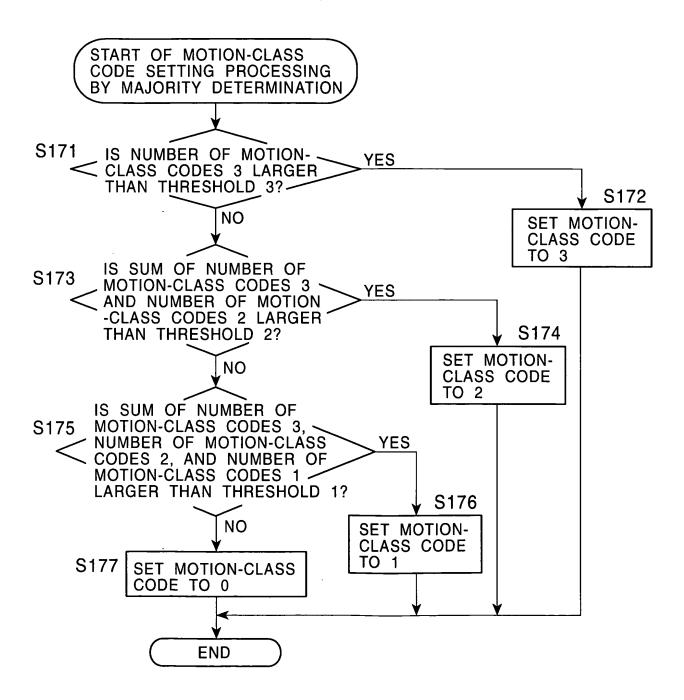


FIG. 58

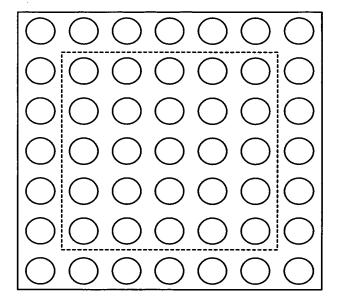


FIG. 59

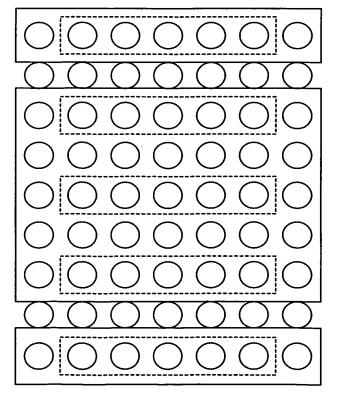


FIG. 60

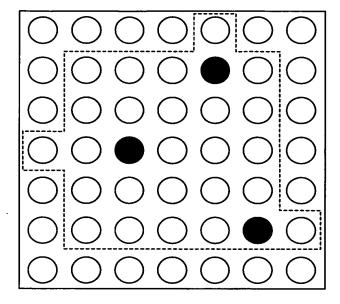


FIG. 61

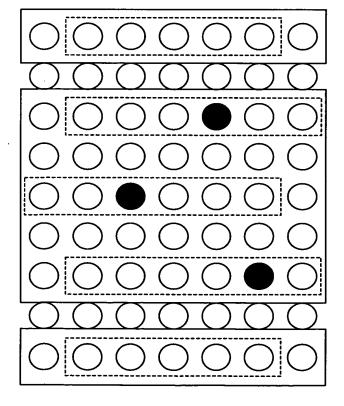
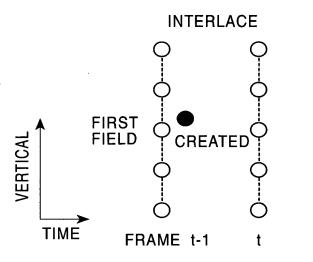


FIG. 62A

FIG. 62C



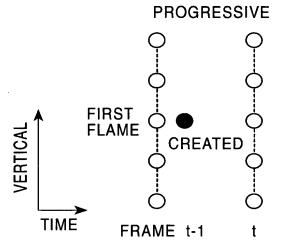
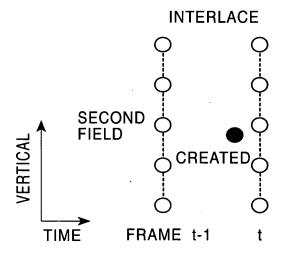
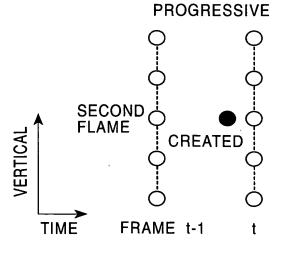


FIG. 62B

FIG. 62D





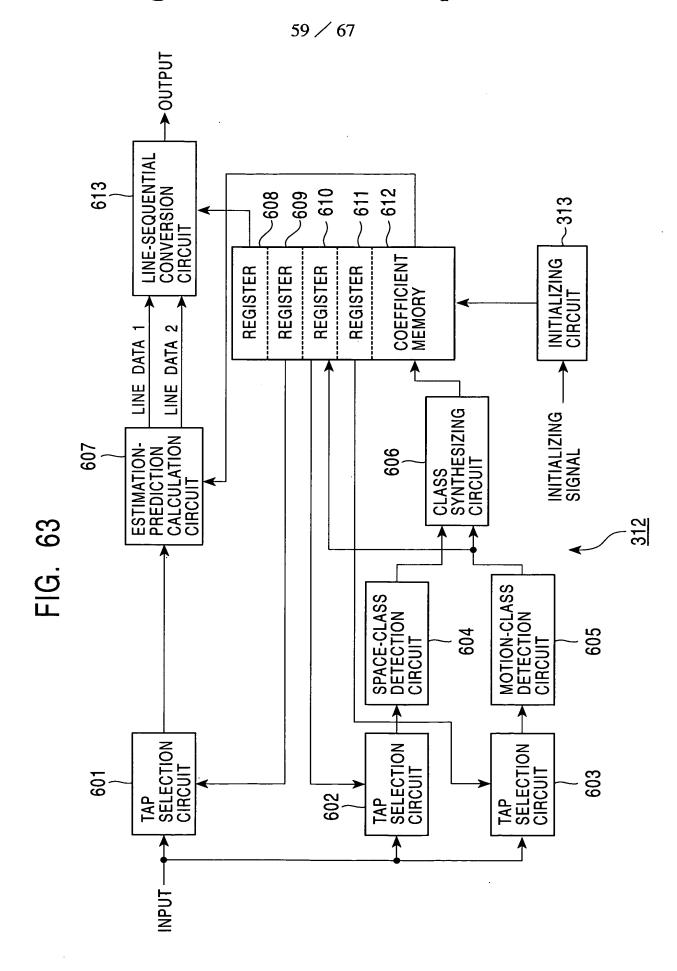


FIG. 64

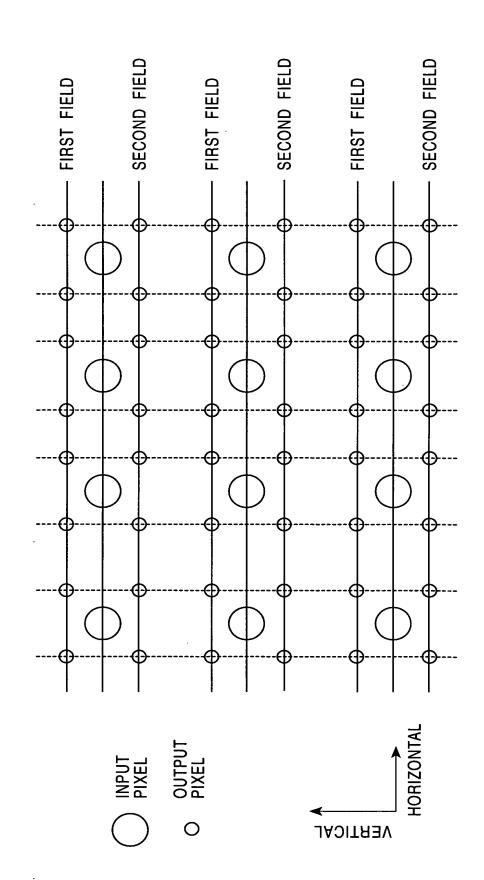


FIG. 65 HORIZONTAL 0 VERTICAL

FIG. 66

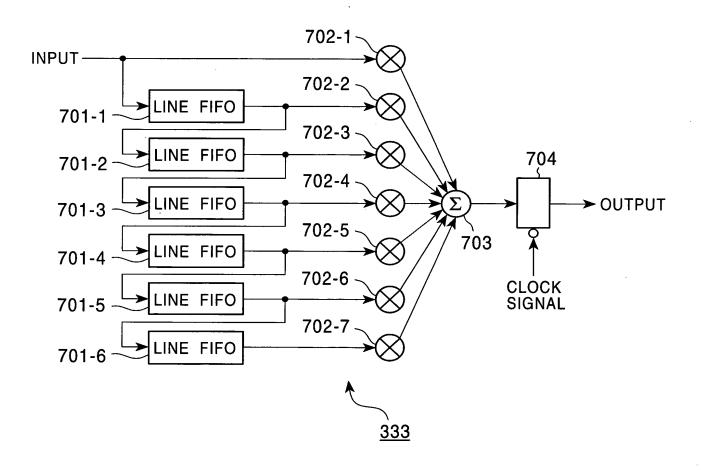


FIG. 67

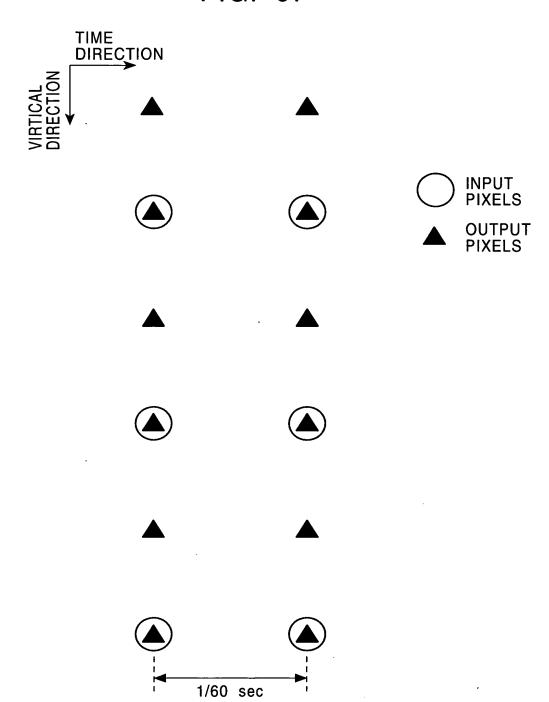
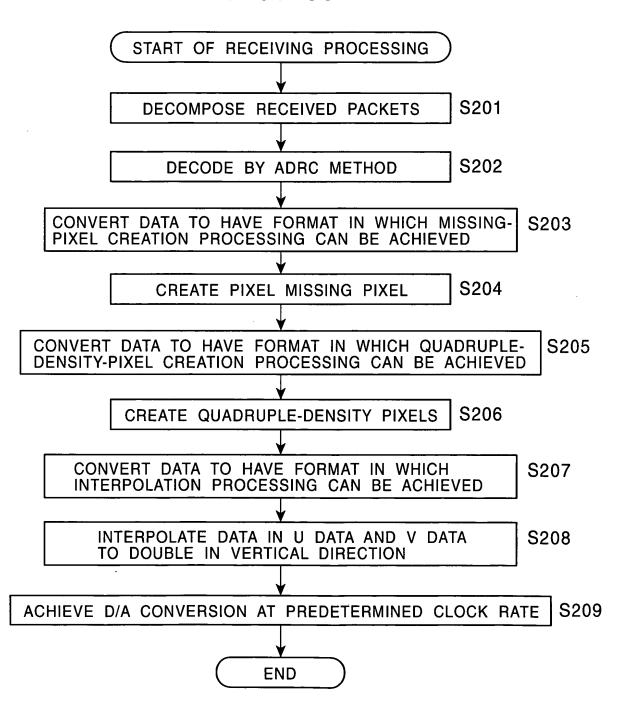


FIG. 68



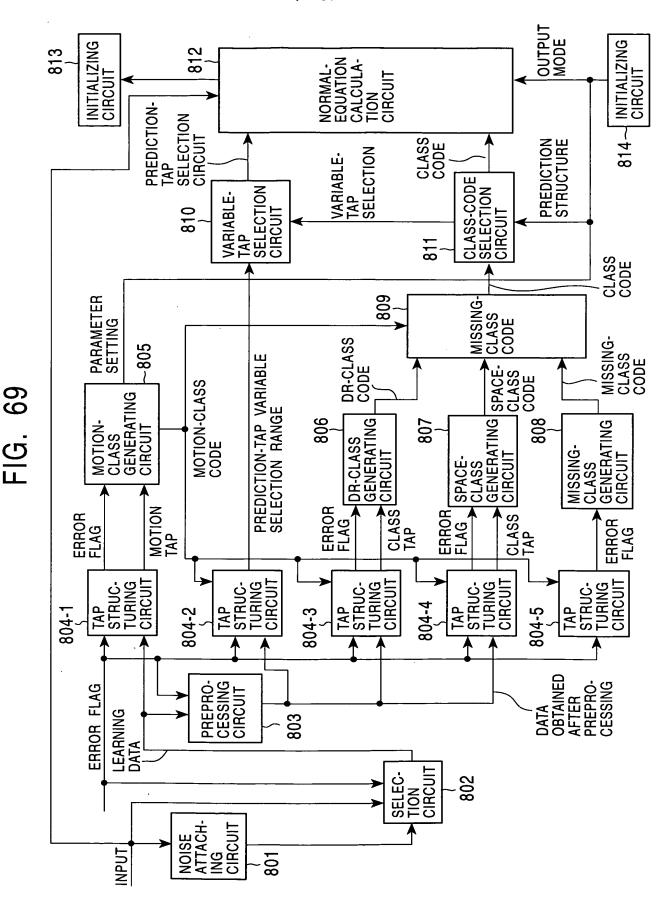


FIG. 70

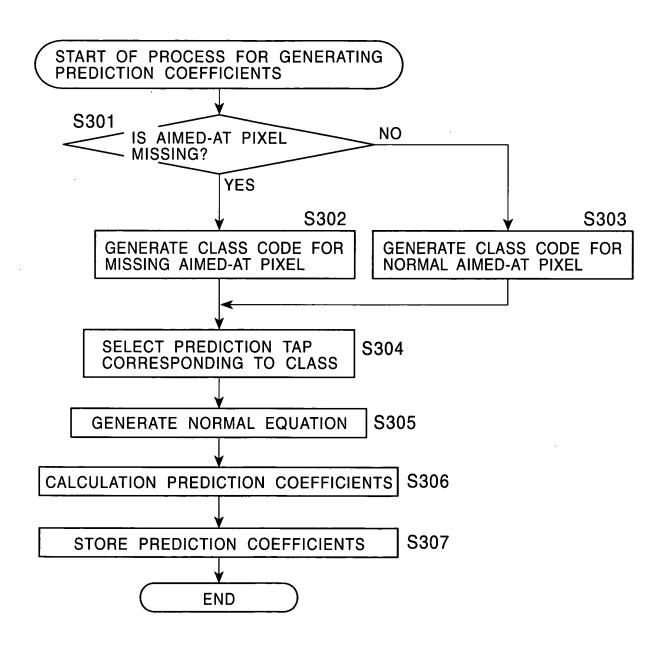


FIG. 71

